Nearest Euclidean Distance Search Associative Memory for High-Speed Pattern Matching

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ABSTRACT

A mixed digital-analog associative memory for Euclidean distance search with fully-parallel processing is reported. Digital processing is used up to subtraction and absolute value calculation in the vector-component comparator part. Analog processing is then applied up to completion of the winner-take-all function. The maximum search time of a test implementation in 0.35 µm CMOS technology having 64 reference patterns, each representing a 16 dimensional vector with 5-bit components, is less than 135 nsec. This is equivalent to 172 GOPS, if a general-purpose 32-bit processor would have to run the same workload.

1. INTRODUCTION

Associative memories have been studied and used as a possible solution for speeding up time-consuming content related searches and for allowing access to data by name or partial content rather than by location or address. In its simplest form, as represented in Fig. 1, an associative memory can be viewed as a hardware device consisting of *N* fixed-size cells, each being marked as empty or storing a data word or record. When presented with a search key and a mask specifying the relevant fields of the stored words, the associative memory responds by marking all the words that match the specified key or, more generally, satisfy the search requirements. An associative memory based system can perform recognition by calculating the distances between input patterns and stored reference patterns. As a measure to express the differences between input data and reference data, the term "distance" is used. The reference pattern with minimum distance is referred to as the "winner" and the reference pattern with the next smallest distance is referred to as the "nearest-loser". Architectures for fully-parallel winner-search according to the Hamming distance [1] and the Manhattan distance [2] have been proposed. Both Hamming and Manhattan distances can be represented by,

$$D = \sum_{i=1}^{W} |S_i - R_i|$$

Where, $S = \{S_1, S_2, \ldots, S_W\}$ and $R = \{R_1, R_2, \ldots, R_W\}$ are input and reference data, respectively. D is called the Hamming distance, when S_i and R_i are 1-bit binaries. D is called the Manhattan distance, when S_i and R_i are k bit binaries ($k > 1$). Digital word-parallel and bit serial associative memories for Hamming distance [3] and Manhattan distance [4] search have also been proposed. Since the complete system is realized as a digital circuit, the size is relatively large compared with [1, 2].

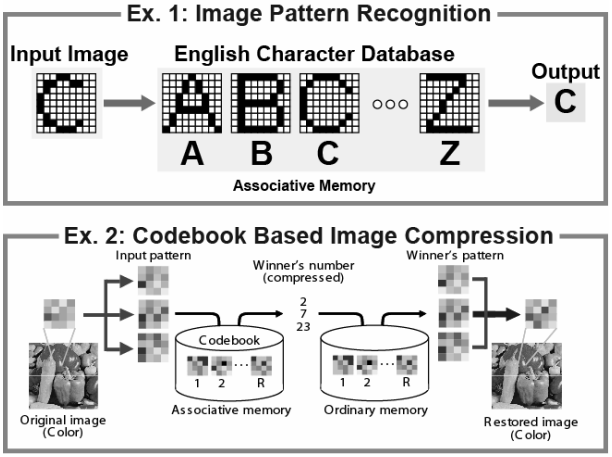

Fig. 1: Application examples of associative memory based system.

However, in many real applications, particularly in the fields of image recognition and authentication, the Euclidean distance is known to give better results than Hamming or Manhattan distance. Euclidean distance is defined by,

$$D_e = \sqrt{\sum_{i=1}^{W} (S_i - R_i)^2}$$

and gives the correct distance between two points in a *W*-dimensional vector space. Unfortunately, the problem of providing an efficient hardware solution for fully-parallel minimum Euclidean distance search is still unsolved.

The most important points for a Euclidean distance hardware implementation are the circuit designs for the square and the square root operations. In particular, the parallel processing for Euclidean distance measurement between the input pattern and many reference patterns,

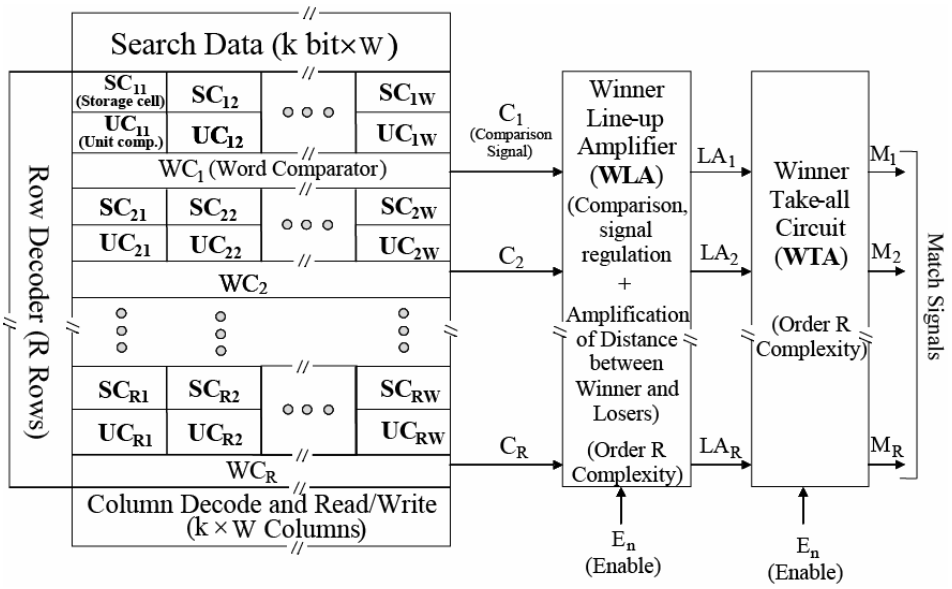

Fig. 2: Block diagram of the mixed digital-analog fully-parallel associative memory for Euclidean distance search.

required for a wide range of applications, is difficult. Here, a solution for fully-parallel winner search capability using Euclidean distance is presented, which consists of mixed digital-analog distance calculation circuitry and an analog winner search circuit and can achieve compact single-chip implementation in conventional CMOS technology as well as short nearest match times up to large distances.

2. ASSOCIATIVE MEMORY ARCHITECTURE AND KEY CIRCUITS

The block diagram of the proposed associative memory with fully-parallel search capability realizing the Euclidean distance measure is shown in Fig. 2. The memory part consists of conventional read / write periphery for storing the reference-data words and for reading out the nearest-match data. A row of the memory field contains *W* storage cells (SC), each with *k* bits plus the circuitry for unit comparison (UC) and word comparison (WC). The word-comparison results C_i are transferred to the winner-search circuit consisting of the winner-line-up amplifier (WLA) and the winner-take-all circuit (WTA). The closely coupled interaction of *WLA* and *WC*s makes it possible to achieve desired maximum amplification of winner-loser distances for all search cases. The outputs signals LA_i of the *WLA* are finally evaluated by the *WTA* to decide on the row, which contains the winner data.

In general, Euclidean distance calculation requires the square as well as the square root operations. In particular, the square root calculation is a hardware expensive operation. To simplify the search problem, it must be first realized that for finding the reference pattern with the minimum Euclidean distance, it is sufficient to compare square distances only. This is because in pattern matching, only comparison of the relative magnitude of the distances is necessary, and this relative magnitude is unaffected by the square root. Therefore, the circuitry for calculating the square roots can be avoided in the minimum Euclidean-distance search problem.

The memory-field structure of the proposed Euclidean distance search hardware is shown in Fig. 3 in more detail. Here, digital *k*-bit subtractor and absolute value calculation units compare the *W* binaries, each with *k*-bit, in all rows of the memory field storing the reference data in parallel with the input data. The digital absolute unit-distance values are then converted into analog currents using current converters (CC). To realize the *CC* function the gates of the *CC*-transistors are connected to the corresponding *k* bit output-signal lines of the unit comparator and their drains are connected together to add the analog currents of all CC transistors. The width of each CC-transistor, $2^{k-1}\times W_0$, varies depending on its bit position in the binary so as to correctly distinguish the weight of each bit. The analog currents from each *CC* are then squared using analog current squarer circuits. The circuit diagram of a simple but efficient analog current squarer circuit is shown in Fig. 4 [5]. It exploits the square-law characteristics of the MOS transistor drain current as a function of the gate voltage, when operated in the saturation region. The advantage of this circuit is that the output current is largely independent of MOS transistor parameters as long as a long channel length is chosen. Finally, the output currents from all squarer circuits are added to get a Euclidean distance-equivalent current, which constitutes the match line current and is fed to the *WLA* for further processing.

For hardware implementation of the Euclidean distance function (without taking the square root), subtractor, squarer, and adder circuits are needed. Due to the flexibility of the analog circuits and also the hybrid structure of some existing associative memory [2, 3] which uses a digital comparator and analog nearest match circuit, two types of implementation for the Euclidean distance function are

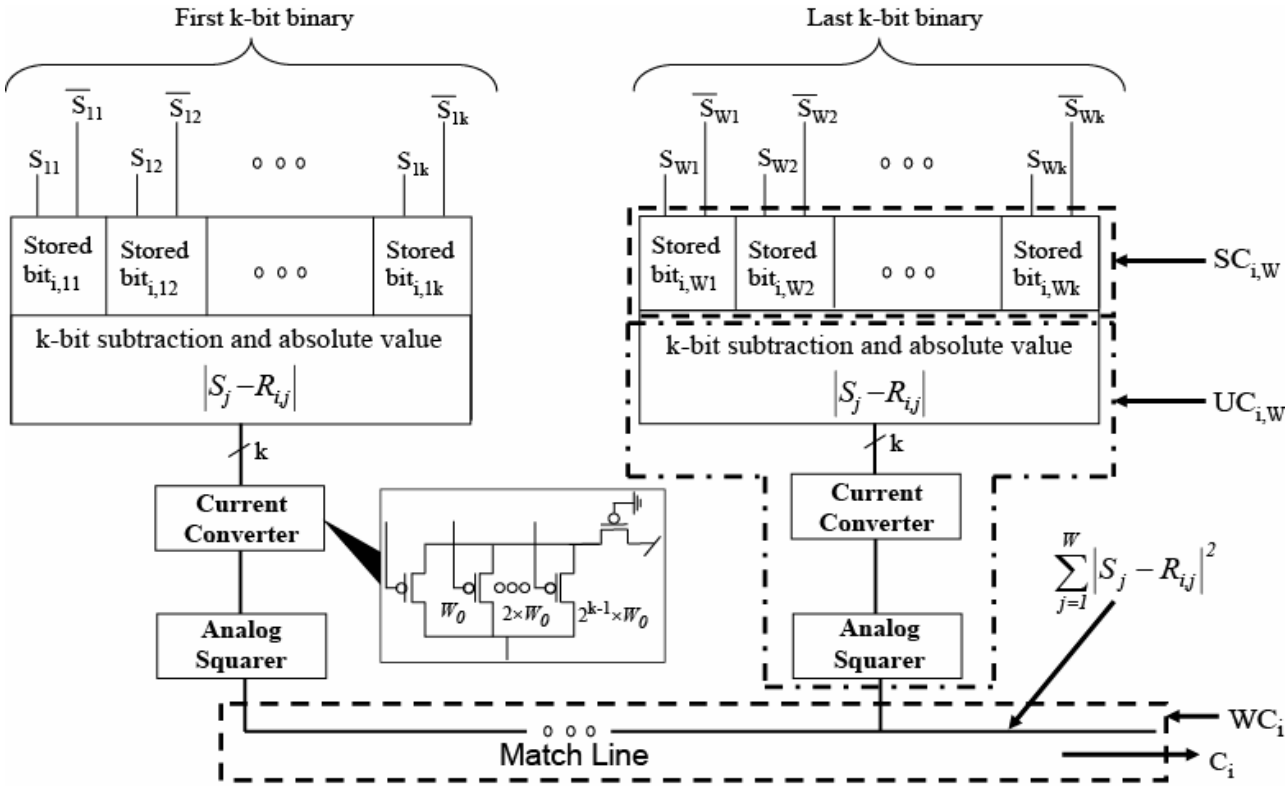

Fig. 3: Architecture concept for an associative memory with fully-parallel minimum Euclidean distance search.

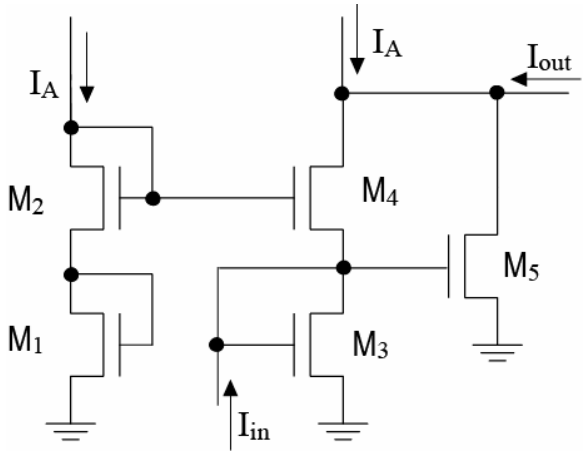

Fig. 4: Analog current squarer circuit used for evaluation of the proposed fully parallel nearest Euclidean distance-search hardware architecture.

possible. One solution is to use a digital squarer circuit and another possibility is to use the analog one. To implement a k bit ($k > 1$) digital squaring circuit, $k(k\text{-}1)$ full adders and k^2 *AND* gates are required (Fig. 5). Each full adder circuit requires at least 22 transistors and each *AND* gate needs at least 6 transistors. Therefore, we need $(28k^2–22k)$ transistors to implement a k-bit digital squarer, which is very expensive for a fully-parallel associative memory architecture. Another drawback of the digital squarer is that its output bit number is twice that of the input bit number. In order to convert the digital distance obtained from the digital squarer to an analog current, the number of transistor increases depending on the number of bits that makes the circuit more complicated. On the other hand, the analog squarer circuit makes the architecture compact because it needs only 5 transistors (Fig. 4), and it does not depend on the number of bits. The proposed architecture uses analog current squarer circuit, which is simple and independent on the input bit size.

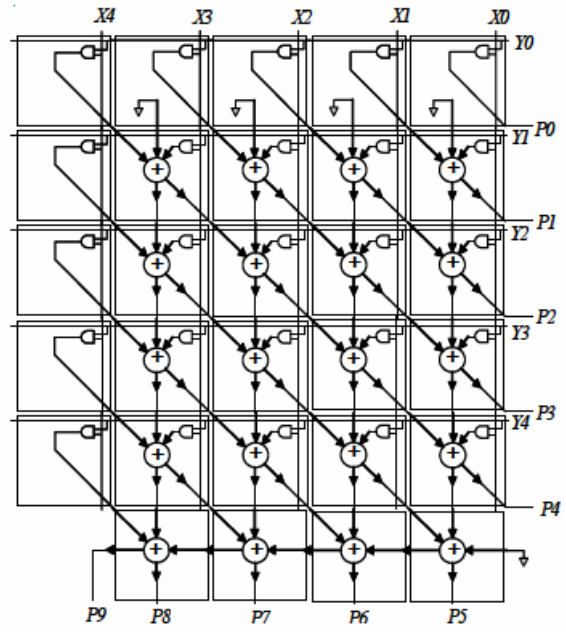

Fig. 5: An example of digital squarer circuit.

The match lines, carrying the Euclidean-distance-equivalent currents, are processed through analog circuits (*WLA*) that pre-amplify the match lines and restrict the large variety of possible analog outputs to a small range by self regulation [2]. The outputs of *WLA*s are then fed to the *WTA* network, which amplifies winner-loser distances by voltage-current-voltage transformations [2].

The final decision circuit in the *WTA* consists of inverters with an adjusted switching threshold. It generates a "1" for the winner row and a "0" for each loser row.

3. SIMULATED PERFORMANCE

Functionality and performance of the proposed nearest Euclidean-distance search associative memory architecture have been evaluated by circuit simulation with a 0.35 μm CMOS technology. The simulated associative memory contains 64 reference patterns with 16 binaries each 5-bit long. This pattern length is sufficient for the application of full-color video-signal compression with 4×4 pixel blocks, after rounding of each color to a 5-bit representation. We have investigated the performance of the circuitry for a very small distance of 1 between winner and nearest loser and the relatively easier distances 2 and 5. Simulated winner-search times, the time periods from rising edge of the enable signal to the winner decision at the output of the winner-take-all circuit, of the designed associative memory as a function of input-winner distance are shown in Fig. 6. Very fast winner search times between 109 and 135 nsec at a relatively small average power dissipation of less than 220 mW are obtained. We have also simulated the system for different MOS device parameter combinations of slow, typical and fast and got similar results. The search time variations are shown as vertical bars in Fig. 6 for winner-nearest loser distance = 1 and amount up to 8.85%. In some cases when both pMOS and nMOS parameters are slow the system failed to output winner for higher input-winner distances and small winner nearest loser distance.

4. CONCLUSION

An associative memory architecture realizing fully-parallel nearest Euclidean-distance search has been proposed. In this architecture we have used a mixed digital-analog Euclidean-distance calculation circuit with an analog current squarer as a key element as well as a fast analog winner search circuit. We have verified the architecture performance by circuit simulation for a 0.35 μm CMOS technology and obtained short search times < 135 nsec, equivalent to a 32-bit processor with 172 GOPS, at low power dissipation of less than 220 mW. These performance data are sufficient even for application in high-performance real-time systems such as feature extraction, pattern matching and image/data compression etc.

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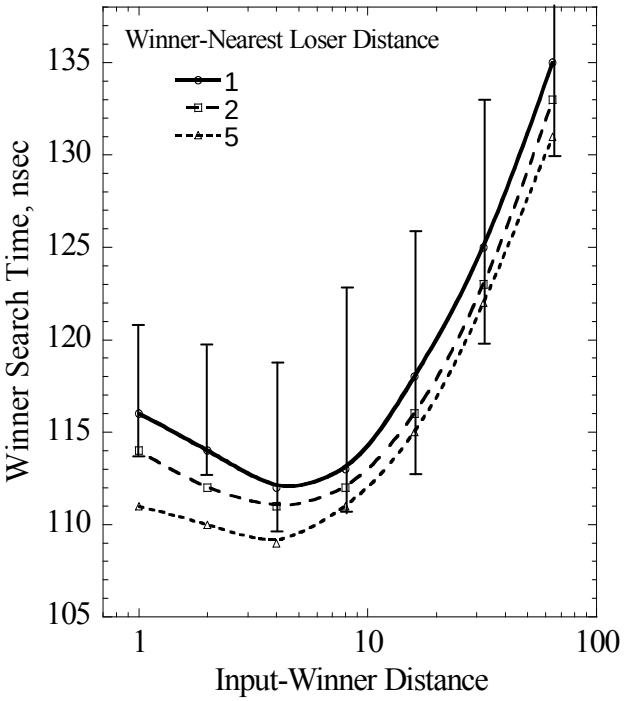

Fig. 6: Winner search time according to the Euclidean distance measure as a function of input-winner distance for different winner-nearest loser distances.

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